computer knowledge-computer organization mcq test-paper6

This unit performs arithmetic logic operations on data values stoered in registers.

A Control unit
B ALU
C Register Set
D Microprocessor

Answer : B

Memory unit accessed by content is called

A Read only memory
B Programmable Memory
C Virtual Memory
D Associative Memory

Answer : D

The instruction 'ORG O' is a

A Machine Instruction
B Pseudo instruction
C High level instruction
D Memory instruction

Answer : B

The sequence of operation in CPU is controlled by

A Control Unit
B ALU
C IC
D Memory

Answer : A

The BSA instruction is

A Branch and store accumulator
B Branch and save return address
C Branch and shift address
D Branch and show accumulator

Answer : B

Control Units are designed using which of the following approach?

A Hardwired approach

B Microprogramming approach

C Both a & b

D None of the above

Answer : C

MIMD stands for

A Multiple instruction multiple data

B Multiple instruction memory data

C Memory instruction multiple data

D Multiple information memory data

Answer : A

What is the full form of CMBR?

A Control Memory Buffer Register

B Condition Memory Buffer Register

C Control Memory Biased Register

D Conditional Memory Biased Register

Answer : A

The time interval between adjacent bits is called the

A Word-time

B Bit-time

C Turn around time

D Slice time

Answer : B

A group of bits that tell the computer to perform a specific operation is known as

A Instruction code

B Micro-operation

C Accumulator

D Register

Answer : A

The I/O Devics are also known as

A Framework

B Peripherals

C Firmware

D irmware

Answer : B

An instruction pipeline can be implemented by means of

A LIFO buffer
B FIFO buffer
C Stack
D None of the above

Answer : B

The mode of data transfer in which sending and receiving units are enabled with same clock is

A Synchronous
B Asynchronous
C Both a & b
D none of these

Answer : A

Main measurement of CPU performance is/are

A execution time
B throughput
C both of the above
D none of the above

Answer : C

The performance of cache memory is frequently measured in terms of a quantity called

A Miss ratio
B Hit ratio
C Latency ratio
D Read ratio

Answer : C

The information available in a state table may be represented graphically in a

A simple diagram
B state diagram
C complex diagram
D data flow diagram

Answer : B

Full form of MIPS is _____

A Millions of Instructions per second
B Millions of Issues per second
C Millions of Indexing per second
D Millions of Interrupt per second

Answer : A

Full form of MFLOPS is _____

A Millions of Fixed Point Operations Per Second
B Millions of Floating Point Operations Per Second
C Millions of Floating Point Opcodes Per Second
D None of the above

Answer : B

Which of the following are parallel computers?

A pipeline computer
B array processor
C multiprocessor system
D All of the above

Answer : D

An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as

A DDA
B DMA
C BR
D Serial interface

Answer : B