

## computer knowledge-vlsi mcq questions-paper1

**VLSI is an acronym for \_\_\_\_?**

- ☐ A Very large Scale Integration
- ☐ B Varying large Scale Integration
- ☐ C Varying large Scale Integrity
- ☐ D None of the above

**Answer : A**

**which below option is used form integrated circuit VLSI technology?**

- ☐ A diodes
- ☐ B transistors
- ☐ C switches
- ☐ D triodes

**Answer : B**

**MOSFETs possess \_\_\_\_\_.**

- ☐ A Low packing density
- ☐ B High packing density
- ☐ C Poor packing density
- ☐ D None of the above

**Answer : B**

**Which among the following is a process of transforming design entry information of the circuit into a set of logic equations?**

- ☐ A Simulation
- ☐ B Optimization
- ☐ C Synthesis
- ☐ D Verification

**Answer : C**

**Integrated chip with lesser than 10 transistors is known as \_\_\_\_\_.**

- ☐ A Small-scale integration
- ☐ B Medium-scale integration
- ☐ C Large-scale integration
- ☐ D Very large-scale integration

**Answer : A**

**\_\_\_\_\_ is the fundamental architecture block or element of a target PLD.**

- ☐ A System Partitioning
- ☐ B Pre-layout Simulation
- ☐ C Logic cell
- ☐ D Post-layout Simulation

**Answer : C**

**How many gates are present on each chip for Medium scale integration?**

- ☐ A 3-30
- ☐ B 30-300
- ☐ C 300-3000
- ☐ D All the above

**Answer : B**

**Logic design of VLSI is used \_\_\_\_\_**

- ☐ A LIFO
- ☐ B FIFO
- ☐ C LILO
- ☐ D FILO

**Answer : B**

**In VLSI design, which process deals with the determination of resistance & capacitance of interconnections?**

- ☐ A Floorplanning
- ☐ B Extraction
- ☐ C Placement & Routing
- ☐ D Testing

**Answer : B**

**Which type of MOSFET exhibits no current at zero gate voltage?**

- ☐ A Depletion MOSFET
- ☐ B Enhancement MOSFET
- ☐ C Both A & B
- ☐ D None of the above

**Answer : B**

**The metal preferred in VLSI for contacting is \_\_\_\_\_.**

- ☐ A Antimony
- ☐ B Aluminum
- ☐ C Germanium

☐ D Silicon

**Answer : B**

**Which type of simulation mode is used to check the timing performance of a design?**

☐ A Behavioural

☐ B Switch-level

☐ C Gate-level

☐ D Transistor-level

**Answer : C**

**Doping can also be done by using \_\_\_\_\_.**

☐ A Contact metallization

☐ B Ion implantation

☐ C Oxidation

☐ D Diffusion

**Answer : B**

**In the simulation process, which step specifies the conversion of VHDL intermediate code so that it can be used by the simulator?**

☐ A Compilation

☐ B Elaboration

☐ C Initialization

☐ D Execution

**Answer : B**

**MOSFET is a \_\_\_\_\_ device.**

☐ A Uni-polar

☐ B Bipolar

☐ C Complementary

☐ D Supplementary

**Answer : A**

**The VLSI design flow starts with:**

☐ A RTL synthesis

☐ B Library mapping

☐ C Product specifications

☐ D None of the above

**Answer : C**

**Register transfer level description specifies all of the registers in a design & \_\_\_\_\_ logic between them.**

- ☐ A Sequential
- ☐ B Combinational
- ☐ C Both a and b
- ☐ D None of the above

**Answer : B**

**Which model is used for scaling?**

- ☐ A constant electric and voltage scaling
- ☐ B constant current model
- ☐ C constant voltage scaling
- ☐ D constant electric scaling

**Answer : A**

**Which is the high level representation of VLSI design?**

- ☐ A Logic design
- ☐ B Functional design
- ☐ C HDL program
- ☐ D Problem statement

**Answer : D**

**Depletion mode n MOSFETs have \_\_\_\_\_ threshold voltage.**

- ☐ A Positive
- ☐ B Negative
- ☐ C Zero
- ☐ D None of the above

**Answer : B**